Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.050”**

**.050”**

**ANODE**

**.034 x .034”**

**Top Material: Au**

**Backside Material: Au**

**Bond Pad Size: .034” X .034”**

**Backside Potential: CATHODE**

**Mask Ref: CPD24**

**APPROVED BY: DK DIE SIZE .050” X .050” DATE: 9/1/21**

**MFG: CENTRAL SEMI THICKNESS .011” P/N: 1N4944**

**DG 10.1.2**

#### Rev B, 7/19/02